AMENDMENT TO THE SPECIFICATION

[022] Further, as shown in Fig. 1, signal traces 120 in the layer 102 route signals from the devices 130 to other points on the circuit board 100. Some of the signal traces 120 connect input/output (I/O) pins of the devices 130 to via pads 122 and 124. The via pads 122 and 124 are in turn connected to vias 126 and 128, respectively, which are passed generally vertically through the multiple layers of the circuit board 100. The vias 126 and 128 are through-hole vias that extend through the layers of the circuit board 100 from one side to another side. Because of a relatively large number of active devices and a relatively large numbers of input/output pins on the active devices, the number of through-hole vias used in the circuit board 100 can be relatively large. In accordance with some embodiments of the invention, embedded decoupling capacitors, such as those in the core assembly 107, are aligned along a direction that is generally perpendicular to a main surface 103 of the circuit board 100. By aligning the embedded capacitors, regions between spaced apart embedded capacitors are defined to provide more space through which the through-hole vias can extend. Aligning capacitors along a given direction refers to lining up the capacitors along the given ~~detection~~ direction such that the capacitors substantially overlap when viewed along the given direction. This allows multiple lines of capacitors to be formed, with one line of capacitors spaced apart from another line of capacitors. The regions between the spaced apart lines of capacitors can be used for through-hole vias.